Gianluca Bellocchi

Curriculum Vitæ et Studiorum

Email
ORCID
Scholar
GitHub
Linkedin

Career

Work career

2/2020 – *Today* : **Research assistant (ING-INF/05)**, *HiPeRT Lab*, UNIMORE, Modena, Italy
Topics: System-level design, heterogeneous SoCs, RISC-V, hardware accelerators, FPGA
Advisor: Prof. Andrea Marongiu
Co-advisor: Dr. Alessandro Capotondi

Visiting experiences

9/2021 – 3/2022 : **Visiting researcher**, *Integrated Systems Laboratory*, ETH Zürich, Zürich, Switzerland
Topics: Design space exploration, heterogeneous SoCs, RISC-V, hardware accelerators, FPGA/ASIC
Ref: Prof. Luca Benini

1/2018 – 6/2018 : **Erasmus exchange student**, Mid Sweden University, Sundsvall, Sweden
Topics: Embedded system design (FPGA, μ-controllers), PCB prototyping, wireless systems
Refs: Prof. Mattias O´Nils, Prof. Luigi Rovati

Conferences

9/2021 : **24th Euromicro Conference on Digital System Design (DSD)**, Palermo, Italy
Contribute: "A RISC-V-based FPGA Overlay to Simplify Embedded Accelerator Deployment"

Workshops

1/2024 : **18th HiPEAC Workshop on Reconfigurable Computing (WRC'2024)**, *Technical University of Munich (TUM)*, Munich, Germany
Contribute: "A System-Level Design Methodology for RISC-V Accelerator-Rich SoCs"
Event: HiPEAC Conference 2024

9/2022 : **7th Italian Workshops on Embedded Systems (IWES 2022)**
Contribute: "An Open-source Design Methodology for the Design Space Exploration of Accelerator-Rich Embedded Systems"

5/2022 : **Spring 2022 RISC-V Week**, Paris, France
Contribute: "Agile Design Methodology for Accelerator-Rich Cluster-based RISC-V SoC"

12/2021 : **6th Italian Workshops on Embedded Systems (IWES 2021)**
Contribute: "An Open-Source Overlay for Reconfigurable, Accelerator-Rich Embedded Systems"

2/2021 : **5th Italian Workshops on Embedded Systems (IWES 2020)**
Contribute: "A RISC-V-based FPGA Overlay to Simplify Accelerator Deployment for Unmanned Vehicles"

Competitions

6/2023 : **AMD OpenHW Competition 2023**
Repository: https://github.com/gbellocchi/xil_open_hw_23

Education

University

9/2017 – 12/2019 : **M.Sc., Electronic Engineering (LM-29)**, *Department of Engineering "Enzo Ferrari"*, UNIMORE, Modena, Italy
Thesis title: "Characterization and performance improvement of a pupillometer prototype for flicker annoyance measurement"
Advisor: Prof. Luigi Rovati

9/2014 – 10/2017 : **B.Sc., Electronic Engineering (270/04)**, *Department of Engineering "Enzo Ferrari"*, UNIMORE, Modena, Italy
Thesis title: "Techniques for data communication between vehicle and vehicle and between vehicle and infrastructure"
Advisor: Prof. Giorgio Matteo Vitetta

Summer schools

7/2024 : **HiPEAC ACACES 2024**, *20th International Summer School on Advanced Computer Architecture and Compilation for High-performance Embedded Systems*, Fiuggi, Italy
Topics: Memory systems and memory-centric computing, compilers, edge AI and methodologies for neural networks deployment on RISC-V multi-core processors
Contribute: "NuNoC: Enhancing a RISC-V-based Heterogeneous SoC with an AXI4-compliant Network-on-Chip featuring QoS control capability"

7/2023 : **HiPEAC ACACES 2023**, *19th International Summer School on Advanced Computer Architecture and Compilation for High-performance Embedded Systems*, Fiuggi, Italy
Topics: Design of RISC-V vector CPUs, HPC programming, neuromorphic computing and machine learning for micro-architectural prediction
Contribute: "Richie: a Framework for Agile Design and Exploration of Accelerator-Rich Cluster-based RISC-V SoC"

Technical training

10/2020 : **Drone Workshop**, *Integrated Systems Laboratory*, ETH Zürich, Zürich, Switzerland
Activity: Introductory concepts and hands-on regarding the Crazyflie 2.1 nano quadcopter platform and suite, ranging from its hardware-software stack, programming ecosystem (SDK, FreeRTOS), deployment tools (neural network) and expansion decks (PULP-shield, AI-deck).

2/2020 – 3/2020: **Xilinx Ultra96 Technical Training Courses**, *Avnet Silica Team*, Italy
Activity: Set of four trainings concerning the full-stack development of embedded FPGA-based MPSoC (Zynq UltraScale+) solutions, ranging from hardware-software co-design (IPs, accelerators, embedded Linux, firmware), components integration (sensors) and application deployment (deep learning).

Publications

Journal articles

[Bel+ew] **Bellocchi, Gianluca**, Alessandro Capotondi, Luca Benini, and Andrea Marongiu. "Richie: A Framework for Agile Design and Exploration of RISC-V-based Accelerator-Rich Heterogeneous SoCs". In: (Under review).

Conference articles

[Bel+21] **Bellocchi, Gianluca**, Alessandro Capotondi, Francesco Conti, and Andrea Marongiu. "A risc-v-based fpga overlay to simplify embedded accelerator deployment". In: *2021 24th Euromicro Conference on Digital System Design (DSD)*. IEEE. 2021, pp. 9–17.

Quanto dichiarato nel presente curriculum vitae corrisponde al vero ai sensi degli artt. 46 e 47 del D.P.R. 445/2000.

August 29, 2024 Gianluca Bellocchi