Curriculum Vitæ et Studiorum

Nome Andrea Marongiu
Email andrea.marongiu@unimore.it
Web http://personale.unimore.it/rubrica/dettaglio/amarongiu
Ufficio MO18-002-027 - Math Building
Department of Physics, Informatics and Mathematics (FIM)
University of Modena and Reggio Emilia
Via Campi, 213/B - 41125 Modena, Italy
Tel.: +39 059 205 5186

Short Bio

Andrea Marongiu received his PhD in Computer, Electronics and Telecommunications Engineering from the University of Bologna, Italy, in 2010. He has been a *postdoctoral reserch fellow* at ETH Zurich, Switzerland, and an *Assistant Professor (RTD A)* at the University of Bologna, Department of Computer Science and Engineering (DISI). He currently holds an **Associate Professor** position at the University of Modena and Reggio Emilia, Deparment of Physics, Informatics and Mathematics (FIM). He is the **Coordinator of the PhD Course in *Computer and Data Science for Technological and Social Innovation*** at the University of Modena and Reggio Emilia. His research interests focus on programming models and architectures in the domain of heterogeneous multi- and many-core systems on a chip (MPSoC). This includes language, compiler, runtime and architecture support to efficiently address performance, predictability, energy and reliability issues in parallel, embedded systems, as well as HW-SW co-design of accelerator-based MPSoCs. In this field, **he has published more than 120 papers in international peer-reviewed conferences and journals, with more than 2000 citations and an *h*-index of 29 [Google Scholar]**. He has collaborated and collaborates with several international research institutes and companies

Contents

Career and Education

CAREER

12/2018 – today

Associate Professor at the Department of Physics, Informatics and Mathematics (FIM), University of Modena and Reggio Emilia, Italy.

10/2017 – 11/2018

Assistant Professor (RTD A) at the Department of Computer Science and Engineering (DISI), University of Bologna, Italy.

10/2013 – 09/2017

Postdoctoral Research Associate at the Department of Information Technology and Electrical Engineering (D-ITET), Swiss Federal Institute of Technology in Zurich (ETHZ), Switzerland.

09/2015 – 09/2017

Research Consultant at the Department of Electrical, Electronic and Information Engineering (DEI), University of Bologna, Italy.

05/2010 – 08/2015

Postdoctoral Research Associate at the Department of Electrical, Electronic and Information Engineering (DEI), University of Bologna, Italy.

EDUCATION

- Abilitazione scientifica nazionale (I fascia), 09/H1 - SISTEMI DI ELABORAZIONE DELLE INFORMAZIONI (15/06/2023) (art. 16, comma 1, Legge 240/10);

- Abilitazione scientifica nazionale (II fascia), 09/H1 - SISTEMI DI ELABORAZIONE DELLE INFORMAZIONI (04/04/2017) (art. 16, comma 1, Legge 240/10);

- Ph.D. degree in Electronics, Telecommunications and Information Technologies Engineering from the University of Bologna, Italy (06/05/2010);
  Thesis Title: *Tecniche di ottimizzazione del software per sistemi su singolo chip per applicazioni di Nomadic Computing*,
  Advisor: *Prof. Luca Benini*

- *Laurea Degree (V.O.)* in Electronic Engineering, from the University of Cagliari, Italy (A.A. 2004/2005)
  Thesis Title: *Progetto e implementazione di un sistema di partizionamento hardware/software per architetture riconfigurabili*,
  Advisor: *Prof. Luigi Raffo, Prof. Salvatore Carta*

VISITING EXPERIENCES

- Visiting researcher at NVIDIA Corporation - USA, Santa Clara (CA) (06/2016)
- Visiting researcher at Brown University - Dept. of Electronics, Providence, Rhode Island, United States [Ref. Prof. Iris R. Bahar, Prof. Maurice Herlihy] (11/2010 - 05/2011)
- Visiting researcher at INRIA Futurs - Parc Orsay Université, Orsay Cedex France [Ref. Albert Cohen] (07/2008 - 09/2008)

Professional Activities

Participation in National and International Research Projects

- *PRIN2022-E53D23007800006-SPACE: Simplifying Predictable and Energy-Efficient Acceleration from Cloud to Edge* [10/2023 –]
  Role: Unit Leader
  Activities: The adoption of heterogeneous Systems-on-chip (SoC) combining multi-core CPUs and FPGA accelerators in the context of *FOG computing* is barred by the complexity of integration and development processes. The SPACE project aims at defining an integrated methodology and design framework to efficiently deploy distributed multi-SoC systems capable of delivering high performance, predictable execution time and limited energy consumption. .

- *HORIZON-CL4-2022-HUMAN-02-02-DAIEDGE: A network of excellence for distributed, trustworthy, efficient and scalable AI at the Edge*
  [09/2023 –] https://daiedge.eu/
  Role: Unit Leader
  Activities: The vision of the dAIEDGE Network of Excellence (NoE) is to strengthen and support the development of the dynamic European AI edge ecosystem under the umbrella of the European AI Lighthouse, and to support advanced research and innovation in distributed AI at edge as essential, enabling and emerging digital technologies across a broad range of industry sectors. dAIEDGE aims to strengthen research and innovation value chains to accelerate digital and green transitions through cutting-edge advanced AI technologies, applications and innovations, building on Europe's existing resources and industrial strengths.

- *H2020-ECSEL-2020-101007326-AI4CSM: Automotive Intelligence for/at Connected Shared Mobility*
  [05/2021 –] https://ai4csm.automotive.oth-aw.de/
  Role: Unit Leader
  Activities: The project has the overall objective of accelerating the transition towards a sustainable green and digital economy. In order to align with the EU Green Deal objectives, which will focus on the creation of an intelligent, competitive, safe, accessible and affordable transport system, the AI4CSM project will develop components for the next generation of autonomous vehicles . The research activities carried out at UNIMORE under the guidance of Andrea Marongiu focus on the development of: (i) a monitoring system based on FPGA acceleration of the attention conditions of the driver of a conditionally automated vehicle; (ii) a system of *monitoring* and control of the use of shared resources of the FPGA computing system aimed at guaranteeing the predictability of the system.

- *H2020-ECSEL-2018-826610-COMP4DRONES: Framework of key enabling technologies for safe and autonomous drones' applications*
  [10/2019 – 01/2023] https://www.comp4drones.eu/
  Role: Unit Leader
  Activities: The project investigates safe software and hardware solutions for drones, in line with the objectives of SESAR – the EU Joint Undertaking on air traffic management research. The goal is to build an ecosystem that will support the systematization and security of drone platforms, with use cases in five sectors: transport, construction, surveillance and inspection, logistics and agriculture. The research activities carried out at UNIMORE under the guidance of Andrea Marongiu focus on the study of design techniques for high-performance computing systems based on system-on-chip with FPGA. Specifically, to simplify the *deployment* of *accelerator-rich* platforms on FPGAs, an *overlay* architecture will be developed that allows the *plug-and-play* integration of accelerators developed with various methodologies and programmable via OpenMP.

- *H2020-FETPROACT-732631-OPRECOMP: Open transprecision computing*
  [01/2017 – 11/2018] http://oprecomp.eu/
  Role: Research Team Leader, Technical Contributor, Co-applicant
  Activities: The project explores a new computing paradigm (*transprecision computing*) aimed at improving the energy efficiency of computing systems by relaxing the accuracy of variables and program parts in order to provide only the necessary precision (as opposed to the "conservative" precision provided by the standard types of the language). The research activities carried out at UNIBO under the guidance of Andrea Marongiu focus on the study of code generation techniques to: i) facilitate the use of hardware "transprecision" for configurable arithmetic precision control; ii) combine data allocation techniques with the abstraction of memory areas configurable in energy/precision, where voltage scaling techniques on on-chip memories can drastically reduce consumption at the cost of a greater probability of error (*bit-flip*).

- *H2020-ICT-688860-HERCULES: High-performance real-time architectures for low-power embedded systems*
  [01/2016 – 01/2019] http://hercules2020.eu/
  Role: Work-Package Leader, Research Team Leader, Co-applicant
  Activities: The project aims to achieve predictable performance in commercial multi-core embedded systems (e.g., GPU). This is to allow their use in systems with real-time constraints such as self-driving cars, at the same time enabling a reduction in energy consumption by an order of magnitude compared to existing prototypes. The research activities carried out at ETHZ under the guidance of Andrea Marongiu focus on the development of compiler and runtime system techniques to guarantee the predictable execution of typical autonomous navigation workloads (computer vision, machine learning, image processing).

- *FP7-ICT-611016-P-SOCRATES: Parallel Software Framework for Time-Critical Many-core Systems*
  [10/2013 – 01/2017] http://www.p-socrates.eu/
  Role: Work-Package Leader, Research Team Leader, Co-applicant
  Activities: The project aims to enable the efficient execution of applications with high performance requirements and real-time constraints on heterogeneous many-core embedded systems, ensuring their predictability and facilitating their programmability. The research activities carried out at ETHZ under the guidance of Andrea Marongiu focus on two fronts. First, on the development of an efficient runtime system for the execution of *OpenMP tasking* parallelism and on the extensions of the OpenMP execution model that allow its analysis using real-time scheduling techniques. Second, on the exploration of architectural extensions (based on FPGA emulation) that facilitate the adoption of shared virtual memory paradigms in heterogeneous systems.

- *FP7-ICT-288574-VIRTICAL: SW/HW extensions for virtualized heterogeneous multicore platforms*
  [07/2011 – 10/2014]
  Role: Work-Package Leader, Research Team Leader, Co-applicant
  Activities: The project aims to study hardware and software extensions for the virtualization of heterogeneous embedded systems based on parallel accelerators. The research activities carried out at UNIBO under the guidance of Andrea Marongiu focus on the development of extensions to the OpenMP programming model to simplify the programmability of accelerators in a shared virtual memory system.

- *FP7-ICT-248776-PRO3D: Programming for Future 3D Architecture with Many Cores*
  [01/2010 – 12/2012]
  Role: Research Team Leader, Technical Contributor, Co-applicant
  Activities: The project aims to study 3D memory stacking technologies as a paradigm for the design of many-core architectures, and the software methodologies necessary to simplify their programmability. The technical contribution is aimed at i) developing compiler methodologies for automatic data partitioning in the 3D distributed memory hierarchy, considering a *partitioned global address space* (PGAS)

model; ii) develop parallel simulation methodologies of target systems on general-purpose GPU architectures.

- *FP7-ICT-224170-SHARE: Sharing Open Source Software Middleware to improve industry competitiveness in the embedded systems domain (CSA)*
  [05/2008 - 04/2010]
  Role: Work-Package Leader, Technical Contributor
  Activities: The project consists of a support action aimed at promoting the diffusion and adoption of open-source software. The technical contribution concerns i) collaboration in the creation of a web-based tool for the evaluation of existing open-source software in a comparative manner; ii) the organization of dissemination events and workshops to promote the initiative.

- *FP7-IDEAS-ERC-291125-MULTITHERMAN: Multi-Scale Thermal Management of Computing Systems*
  [04/2012 – 03/2018] http://wwwmicrel.deis.unibo.it/multitherman
  Role: Technical Contributor, Co-applicant
  Activities: The project studies alternative solutions to the established worst-case design practices in thermal planning/management, through the integration of thermal-aware design methodologies and thermal control based on multi-scale strategies for distributing the computational load. The technical contribution is focused on the development of a distributed runtime system for massively parallel architectures.

- *ARTEMIS-100230-SMECY : Smart Multicore Embedded Systems*
  [02/2010 – 01/2013]
  Role: Task leader, Technical Contributor
  Activities: The project studies new programming technologies aimed at efficiently exploiting parallelism in many-core systems. The technical contribution focuses on language and compilation aspects to improve data locality in a many-core accelerator (ST-P2012/STHORM).

Institutional Charges

- Coordinator of the PhD Course in *Computer and Data Science for Technological and Social Innovation* of the University of Modena and Reggio Emilia (https://www.cds.unimore.it/).

Industrial Collaborations

- Technology Innovation Institute, Abu Dhabi [2020 -]
  Task leader in the context of a commissioned research contract on secure offloading methodologies on a heterogeneous multi-core platform for autonomous drones.

- Magneti Marelli [2016 - 2018]
  Principal Investigator for a commissioned research contract on the comparative acceleration (GPU, MPPA, FPGA) of computational *kernels* extracted from *autonomous driving* applications (*perception*, *planning*, *control*).

- ST Microelectronics [2010-2012]
  Principal Investigator for a commissioned research contract on the integration of *shared-memory* accelerators in the ST P2012/STHORM platform.

- ST Microelectronics [2010-2012]
  Principal Investigator for a commissioned research contract on the development of methodologies and *tools* for the support of the OpenMP programming model on the ST P2012/STHORM platform.

- Freescale Semiconductors Ltd. [2007]
  Collaborator and technical leader for a commissioned research contract on the development of power management techniques at the operating system level (Linux) in mobile devices.

Editorial Boards

- **Guest Editor** for the special issue on *Energy-Quality Scalable Circuits and Systems for Sensing and Computing* of the *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* (vol 8, n.3, 4). The special issue collects contributions on techniques ranging from software to hardware, from circuits to applications, aimed at highlighting the benefits obtainable from the trade-offs between quality (accuracy) of computation and energy consumption.
- **Editor** (and co-author) of the book "High-Performance and Time-Predictable Embedded Computing", River Publishers (https://dx.doi.org/10.13052/rp-9788793609624) which presents recent developments in the field of programming models and development tools for these complex systems, capable of guaranteeing high performance within the imposed time constraints.

Organization of International Conferences and Workshops

Andrea Marongiu is or has been a **member of the Technical Program Committee** per the following international conferences and workshops:

- ICCAD (2023, 2024) - ACM/IEEE International Conference on Computer-Aided Design
- DSD (2021, 2022) - Euromicro Conference on Digital Systems Design
- FDL (2022) - CEDA/IEEE Forum on specification & Design Languages
- DATE (2014 - 2019) - Design Automation and Test in Europe
- MCSoC (2014 - 2018) - International Symposium on Embedded Multicore/Many-core Systems-on-Chip
- SCOPES (2014 - 2018) - International Workshop on Software and Compilers for Embedded Systems
- EUC (2014 - 2015) - International Conference on Embedded and Ubiquitous Computing
- FPL (2015) - International Conference on Field-Programmable Logic and Applications
- DASIP (2013) - Design and Architectures for Signal and Image Processing
- SOMRES (2011) - Workshop on Synthesis and Optimization Methods for Real-Time Embedded Systems

He has been a **member of the organizing committee** of the sixth "International Workshop on Advances in Parallel Programming Models and Frameworks for the Multi-/Many-core Era" (APPMM, @HPCS 2018), of the "Workshop on Vertical Virtualization Techniques in Heterogeneous Multicore Embedded Systems" (VVITEMES, @HIPEAC 2014), of the special session "Hw/Sw acceleration of Vision and Image processing applications for embedded targets" of the international conference "Design & Architectures for Signal & Image Processing' ' (DASIP 2013).

Reviewer for International Journals, Conferences and Workshops

Andrea Marongiu serves or has served as a **reviewer** for numerous other conferences and journals, including:

- *Conferences and Workshops*:

  PACT - Parallel Architectures and Compilation Techniques, LCTES - Languages, Compilers, Tools and Theory for Embedded Systems, ICECS - International Conference on Electronics, Circuits, and Systems, ICS - International Conference on Supercomputing, CASES - International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, CODES - Conference on Design and Architectures for Signal and Image Processing, ASAP - International Conference on Application-specific Systems, Architectures and Processors, HIRES - High-performance and Real-time Embedded Systems.

- *Journals*: IEEE Access IEEE Transactions on Computers (TC), IEEE Transactions on Parallel and Distributed Systems (TPDS), IEEE Transactions on Industrial Informatics (TII), IEEE Transactions on Signal Processing (TSP), IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS),

  ACM Transactions on Embedded Computing Systems (TECS), ACM Transactions on Design Automation of Electronic Systems (TODAES), ACM Transactions on Architecture and Code Optimization (TACO), ACM Transactions on Reconfigurable Technology and Systems (TRETS),

  ELSEVIER Microprocessors and Microsystems: Embedded Hardware Design (MICPRO), ELSEVIER Journal of System Architecture (JSA), ELSEVIER Computers & Electrical Engineering (COMPELECENG), ELSEVIER Journal of Systems and Software (JSS), ELSEVIER Future Generation Computer Systems (FGCS), ELSEVIER Simulation Modelling Practice and Theory (SIMPAT), ELSEVIER Microelectronics Journal (MEJ), ELSEVIER Integration, the VLSI Journal (VLSI), ELSEVIER Journal of Parallel and Distributed Computing (JPDC),

  SPRINGER International Journal of Parallel Programming (IJPP), SPRINGER Journal of Real-Time Image Processing (JRTIP), SPRINGER Artificial Intelligence Review (AIRE), SPRINGER Journal of Supercomputing (JSUPE),

SCIENTIFIC COLLABORATIONS WITH INTERNATIONAL RESEARCH INSTITUTES (HIGHLIGHTS)

- Collaborations with Italian Academic Institutes:
  - Università di Bologna [2010 - ongoing] - Luca Benini
    Tema: Efficient support for OpenMP execution on massively parallel heterogeneous systems.
  - Università di Cagliari/Sassari [2018 - ongoing] - Francesca Palumbo
    Tema: FPGA overlay for accelerating autonomous drone workloads.
  - Università degli Studi dell'Aquila [2018 - ongoing]
    Tema: Memory bandwidth monitoring and regulation in heterogeneous FPGA-based systems.
  - Università di Ferrara [2010 - 2018] - Davide Bertozzi
    Tema: Sistemi MPSoC basati su network-on-chip; fog computing.
  - Politecnico di Torino - [2008 - 2010] - Andrea Acquaviva
    Tema: Management of aging effects (NBTI) in MPSoC systems.

- Collaborations with International Research Institutes:
  - Swiss Federal Institute of Technology (ETHZ) - Switzerland [2013 - ongoing] - Luca Benini
    Tema: Predictable Execution Models and hardware support for heterogeneous systems-on-chip.
  - Istituto Dalle Molle di studi sull'intelligenza artificiale (SUPSI) - Switzerland [2021 - ongoing] - Daniele Palossi
    Tema: Accelerating workloads for autonomous drones and nano-drones.
  - Brown University - Lowell, MA, USA [2018 - ongoing] - Dimitra Papagiannopoulou
    Tema: Transactional memory support in heterogeneous MPSOC systems.
  - Czech Technical University in Prague - Czech Republic [2016 - 2020] - Zdenek Hanzalek
    Tema: Predictable co-scheduling in integrated CPU/GPU SoCs.
  - Barcelona Supercomputing Center - Spain [2013 - 2017] - Eduardo Quiñones
    Tema: Time-predictable OpenMP
  - University of Massachusetts Lowell - Providence RI, USA [2010 - 2017] - Iris R. Bahar
    Tema: Support for transactional memory in MPSOC systems; extensions for variability tolerance.
  - University of California, San Diego - USA [2012 - 2015] - Rajesh Gupta
    Tema: Architectural extensions and programming models for variability-aware task allocation.
  - Universite de Bretagne Sud - Lorient, France [2011 - 2015] - Philippe Coussy
    Tema: Architectures and tools for the integration of hardware generated via HLS in parallel shared-memory clusters.
  - EPFL - Lausanne, Switzerland [2010 - 2012] - David Atienza
    Tema: Accelerated manycore system simulation on GPGPU.
  - EPFL - Lausanne, Switzerland [2009 - 2010] - Giovanni De Micheli
    Tema: Programming model support for QoS in NoC-based MPSoC systems.
  - INRIA Futurs - Orsay Cedex, France [2008 - 2009] - Albert Cohen
    Tema: Compilation techniques for transactional memory support.
  - Penn State University - USA [2006 - 2007] - Mahmut Kandemir
    Tema: Lightweight synchronization support in automatic loop parallelization schemes.

Teaching

September 2023 - now

Titular Professor
Dept. of Law, University of Modena and Reggio Emilia
Bachelor Degree: “Scienze Strategiche”.
Calcolatori Elettronici - *9 credits, 91 hours*.

March 2023 - now

Titular Professor
Dept. of Physics, Informatics and Mathematics, University of Modena and Reggio Emilia
Bachelor Degree in Computer Science.
Linguaggi e Compilatori - *6 credits, 48 hours*.

November 2019 - now

Titular Professor
Dept. of Physics, Informatics and Mathematics, University of Modena and Reggio Emilia
Master Degree in Computer Science.
High Performance Computing - *9 credits, 63 hours*.

March 2020 - now

Titular Professor
Dept. of Physics, Informatics and Mathematics, University of Modena and Reggio Emilia
Bachelor Degree in Computer Science.
Architettura dei Calcolatori - *9 credits, 72 hours*.

November 2019 - February 2021

Titular Professor
Dept. of Physics, Informatics and Mathematics, University of Modena and Reggio Emilia
Bachelor Degree in Computer Science.
Programmazione I - *40 ore*.
Architettura dei Calcolatori - *6 credits, 52 hours*.

February 2018 - September 2019

Titular Professor
Dept. of Computer Science and Engineering, University of Bologna
Master Degree in Computer Engineering
Fondamenti di Informatica T - Modulo 2 - *3 credits, 30 hours*.

September 2016 - September 2017

Adjunct Professor
Dept. of Physics, Informatics and Mathematics, University of Modena and Reggio Emilia
Bachelor Degree in Computer Science.
Programmazione I - *9 credits, 72 hours*.

2013 - 2017

Teaching Assistant
Swiss Federal Institute of Technology in Zurich (ETHZ) - Electronic Engineering - master degree
Advanced System-on-Chip Design.

2013 - 2017

Teaching Assistant
University of Bologna - Master Degree in Electronics and Computer Engineering
Hardware/Software Design Methodologies.

2007 - 2013

Teaching Assistant
University of Bologna - Master Degree in Electronics and Computer Engineering
Metodologie di Progettazione Hardware/Software.

Publications List

Refer to the following links for the most up-to-date publications list:

- Google Scholar
- Scopus
- DBLP

The undersigned declares that what is indicated in this curriculum vitae is true, pursuant to articles 46 and 47 D.P.R. 445/2000.

Date

24.06.2024

Signature