CURRICULUM VITAE OF
ANDREA PADOVANI

1. **CURRICULUM**
2. **RESEARCH ACTIVITIES**

1. CURRICULUM

1978 I was born in Reggio Emilia, Italy, the 09th, December 1978.

2005 I graduated in **Electronic Engineering (M.S.)** at the University of Modena e Reggio Emilia, Italy, with an thesis entitled "Reliability of Future Generation NROM Cells - Analysis and Simulation,". In the months of September and October I collaborate with the Department of Sciences and Method for Engineering of the University of Modena e Reggio Emilia on a project entitled "**Modeling of NROM non-volatile memories**".

2006-2008 I worked through my **Ph.D. in Engineering Science** (**Dottorato di Ricerca in Scienze dell'Ingegneria - XXI ciclo**) at the University of Ferrara, Italy. During these years I collaborated with the Department of Sciences and Method for Engineering of the University of Modena e Reggio Emilia on projects concerning the investigation and modeling of innovative and conventional Flash memories.

2009 In March I defended my Ph.D. thesis, entitled "**Modeling and Reliability of Innovative Flash Memories**" at the University of Ferrara, Italy. My supervisor was Prof. Andrea Chimenton.

2009-2010 Post-Doc position at the Department of Sciences and Method for Engineering of the University of Modena e Reggio Emilia, working on a project entitled "**Future generation charge-trapping non-volatile Flash memories**".

2010-2013 Assistant Professor in Electronics at the INTERMECH center and at the Department of Sciences and Method for Engineering of the University of Modena e Reggio (SSD ING-INF/01).

2014 On February 4th, 2014 I obtained the **National Scientific qualification** as Associate Professor in the Italian higher education system, for the disciplinary field of 09/E3 - Electronics. (Academic Recruitment Field 09/E - Electrical and electronic engineering and measurements, according to the national classification). (https://abilitazione.cineca.it/ministero.php/public/esitoAbilitati/settore/09%252FE3/fascia/2).

2015 I co-founded the Italian start-up MDLab s.r.l., with the aim of developing a commercial software for the simulation of semiconductor devices (subsequently named Ginestra®) focusing on the simulation of charge and atom transport and on the degradation of dielectric materials used in electronic devices.

2016 I have been hired by MDLab s.r.l. as an Application Engineer, position I held until February 2019. In this period I initially dealt with the development of the Ginestra® software, and then focused on its use, both in the context of specific corporate projects and for customer support. I personally managed customer relationships, with numerous visits to their offices (mainly in the United States and Asia).

2017 I co-founded the company MDLSoft Inc. with headquarters in Santa Clara, CA, USA, which took control of the company MDLab s.r.l., with the aim of developing and marketing the commercial software for the simulation of electronic devices Ginestra®.

2019 In February 2019 I have been hired by Applied Materials Italia s.r.l. as *Senior Manager Applications Development* within a group directly employed by the headquarters in Santa Clara, CA, USA which deals with the development and marketing of the Ginestra® software and its use to support the company's core business. As part of this role I led a group of Application Engineers in the development of models that describe the physics and behavior of electronic devices and in the use of the Ginestra® software for: development of use cases,

application to problems of high interest, use for support to external customers (ranging from training to consultancy) and use for internal projects. I held this position until March 2022.

2022 On February 1st, 2022 I renewed the **National Scientific qualification** as Associate Professor in the Italian higher education system, for the disciplinary field of 09/E3 - Electronics. (Academic Recruitment Field 09/E - Electrical and electronic engineering and measurements, according to the national classification). (https://asn21.cineca.it/pubblico/miur/esito-abilitato/09%252FE3/2/1).

2022 On April 1st, 2022 I started working as Assistant Professor (with Tenure Track) at the Enzo Ferrari Engineering Department (DIEF) of the University of Modena and Reggio Emilia (SSD ING-INF/01).

2023 On November 7th, 2023 I obtained the **National Scientific qualification** as Full Professor in the Italian higher education system, for the disciplinary field of 09/E3 - Electronics. (Academic Recruitment Field 09/E - Electrical and electronic engineering and measurements, according to the national classification). (https://asn21.cineca.it/pubblico/miur/esito-abilitato/09%252FE3/1/6).

2025 On April 1st, 2025 I became Associate Professor in electronics at the Enzo Ferrari Engineering Department (DIEF) of the University of Modena and Reggio Emilia (SSD ING-INF/01). On June 1st, 2025 I moved to the Department of Engineering Sciences and Methods (DISMI) of the University of Modena e Reggio Emilia, Reggio Emilia.

1.1 TEACHING ACTIVITIES

2009 I held the course Semiconductor Memories (54 hours) for the Master Degree in Electronic Engineering at the Engineering Department of the University of Modena e Reggio Emilia, Modena, for the academic year 2009/2010.

2010 Docente del modulo da 16 ore “Circuiti di condizionamento del segnale” nell’ambito del progetto “IFTS Tecnico superiore per il disegno e la progettazione industriale di sistemi meccatronici” organizzato dalla scuola per la gestione d'impresa CIS di Reggio Emilia.

2012-2013 I hold course Electronic Devices and Technology (54 hours) for the Master Degree in Mechatronic Engineering at the Dipartimento di Scienze e Metodi dell’Ingegneria of the University of Modena e Reggio Emilia, Reggio Emilia, for the academic years 2011/2012 and 2012-2013.

2013-2015 I held the course of Advanced Electronic Devices (54 hours) for the Master Degree in Electronic Engineering at the Engineering Department of the University of Modena e Reggio Emilia, Modena, for the academic year 2013-2014.

2022 I held the course of Sistemi Elettronici Industriali (81 hours) of the Degree Course in “Ingegneria Gestionale” at the Dipartimento di Scienze e Metodi dell’Ingegneria of the University of Modena e Reggio Emilia, Reggio Emilia for the academic year 2022/2023.
I held the course of Applied Electronics (54 hours) of the Degree Course in “Tecnologie per l'Industria Intelligente” at the Dipartimento di Scienze e Metodi dell’Ingegneria di Reggio Emilia for the academic year 2022/2023.

2023 I held the course of Sistemi Elettronici Industriali (81 hours) of the Degree Course in “Ingegneria Gestionale” at the Dipartimento di Scienze e Metodi dell’Ingegneria of the University of Modena e Reggio Emilia, Reggio Emilia for the academic year 2023/2024.

I held the course of Applied Electronics (63 hours) of the Degree Course in "Tecnologie per l'Industria Intelligente" at the Dipartimento di Scienze e Metodi dell'Ingegneria di Reggio Emilia for the academic year 2023/2024.

2024 I held the course of Sistemi Elettronici Industriali (81 hours) of the Degree Course in "Ingegneria Gestionale" at the Dipartimento di Scienze e Metodi dell'Ingegneria of the University of Modena e Reggio Emilia, Reggio Emilia for the academic year 2024/2025.
I held the course of Applied Electronics (63 hours) of the Degree Course in "Tecnologie per l'Industria Intelligente" at the Dipartimento di Scienze e Metodi dell'Ingegneria di Reggio Emilia for the academic year 2024/2025.

2025 I held half of the course Reliability of Electron Devices (12 hour) at the International Doctorate School in Information and Communication Technologies (ICT) at the University of Modena and Reggio Emilia.

2025 I held the course of Sistemi Elettronici Industriali (81 hours) of the Degree Course in "Ingegneria Gestionale" at the Dipartimento di Scienze e Metodi dell'Ingegneria of the University of Modena e Reggio Emilia, Reggio Emilia for the academic year 2024/2025.
I will held the course of Applied Electronics (63 hours) of the Degree Course in "Tecnologie per l'Industria Intelligente" at the Dipartimento di Scienze e Metodi dell'Ingegneria di Reggio Emilia for the academic year 2025/2026.

I've been supervisor of several master thesis. I've been the supervisor of two Ph.D. students.

2. RESEARCH ACTIVITIES

As per September 16, 2026 Scopus database (Author ID: 17346546300) reports the following bibliometric indexes for Andrea Padovani

- numero di documents: **198**, of which **93** on international journals
- number of citations: **6304**
- h-index: **35**

Google Scholar: https://scholar.google.com/citations?user=0cQPSR4AAAAJ&hl=it
ORCID iD: https://orcid.org/0000-0003-1145-5257

The main focus of my research activities is on the development of physics-based, material related models for the understanding, description and prediction of the operation and reliability of several semiconductor devices. More specifically, my scientific contributions are related to logic transistors (with the development of models describing all the phenomena relevant for gate dielectric stacks, from charge transport/trapping to breakdown), a wide range of non-volatile memory technologies (charge trapping devices, resistive RAMs and ferroelectric devices) and selector devices.
All the research activities that I carried on or supervised have a main common ground: the description and modeling of physics-based phenomena occurring in non-semiconductor materials, mainly (but not only) high-k dielectrics. They have been collected into a unified modeling framework, which subsequently led to the development of the innovative commercial semiconductor device simulation software Ginestra™, capable to fill some of the gaps left by the other commercial products available on the market. Since its introduction in 2015, the Ginestra software has been adopted by many semiconductor companies and is now part of the Applied Materials portfolio (https://www.appliedmaterials.com/eu/en/semiconductor/ginestra-software.html).

In the field of non-volatile memory devices, I initially worked on conventional floating gate devices, planar charge trapping devices (such as NROM and TANOS) and devices that use materials with a high dielectric constant for the engineering of the tunnel barrier in Floating Gate (VARIOT) type structures. In recent years my research activity has mainly focused on the study and modeling of: i) devices based on transition metal oxides (TMO, in particular HfO_2), used both for the development of non-volatile resistive switching

(RRAM) memory technologies and for neuromorphic applications; ii) 3D-NAND type non-volatile charge trapping memory devices; iii) ferroelectric devices such as FeFETs, Ferroelectric Tunnel Junctions (FTJs) and FeRAM. My activities have mainly concerned the understanding and modeling of the physical mechanisms that govern their functioning and degradation.

In the field of logic transistors, I deal with the study and modeling of the physical phenomena underlying the main reliability problems of devices with conventional (SiO_2/SiON) and high dielectric constant (HfO_2) gate dielectrics: gate leakage, Stress-Induced Leakage Current (SILC), Bias Temperature Instabilities (BTI), Random Telegraph Noise (RTN), degradation and breakdown.

In Academia, the activities were carried out in the context of numerous national and international research projects, and in collaboration with semiconductor companies (Saifun Semiconductors, STMicroelectronics, Applied Materials, Samsung, Intel), other universities (Technical University of Munich, Munich, Germany; University College London, London, UK; Tampere University, Tampere, Finland; Stanford University, CA, USA; Nanyang Technological University, Singapore; Singapore University of Technology and Design, Singapore; Gwangju Institute of Science and technology, Gwangju, Republic of Korea; Boise State University, Idaho, USA; Georgia Institute of Technology, Georgia, USA; Purdue University, Indiana, USA; University of California San Diego, San Diego, USA; IIT Bombay, India, IIT Madras, India; National Tsing Hua University, Taiwan;) and international research centers (SEMATECH, USA; IMEC, Belgium; CEA-LETI, France).

Also while working in the Industry, I continued to carry out research activities with four main objectives: i) the development of physical models to be implemented in the Ginestra™ software; ii) to support activities on specific customer projects; iii) support to the core business of the company; iv) European projects. The research activities have been carried out in collaboration with the most important semiconductor companies, universities (Singapore University of Technology and Design, Singapore; Bangladesh University of Engineering and Technology, Bangladesh; Pohang University of Science and Technology, South Korea; University College London, England; Peking University, China; University of Texas at Dallas, USA) and international research centers (IMEC, Belgium; CEA-LETI, France).

I am currently reviewer of several international journals, such as IEEE Transactions on Electrons Devices, IEEE Electron Device Letters, IEEE Transactions on Device and Materials Reliability, Journal of Applied Physics (AIP), Applied Physics Letters (AIP), Microelectronics Reliability (Elsevier), Solid-State Electronics (Elsevier), Journal of Materials Science (Elsevier), Materials Chemistry and Physics (Elsevier), Semiconductor Science and Technology (IOP), Journal of Physics D (IOP) and Nanotechnology (IOP).

Competitive Funding Projects

The research activity carried out both in the academic and industrial fields was partly carried out as part of national and international research projects, including:

1. Work Package leader (WP3) and Coordinator of the Applied Materials Unit of the EU project "INTERSECT - Interoperable Material-To-Device Simulation Box For Disruptive Electronics", funded by the European Union under the Horizon 2020 research and innovation programme (grant agreement No 814487) (https://intersect-project.eu/).
2. Coordinator of the Applied Materials Unit of Work Package 2 of the EU project "iQubits - Integrated Qubits Towards Future High-Temperature Silicon Quantum Computing Hardware Technologies", funded by the European Union under the Horizon 2020 research and innovation programme (grant agreement No 829005) (https://www.iqubits.eu/).
3. Member of the Applied Materials Unit of the EU project "OpenModel - Integrated Open Access Materials Modelling Innovation Platform for Europe", funded by the EU under the Horizon 2020 research and innovation programme (grant agreement No 953167).
4. Member of the University of Modena e Reggio Emilia unit of the il EU project "Attoswitch - Dirac cold-source transistor technologies towards attojoule switching", funded by the EU under the Horizon 2020 (grant agreement No 101135571) (https://www.attoswitch.eu/).
5. FAR 2024, 2023 and 2022 of the Engineering Department "Enzo Ferrari", University of Modena and Reggio Emilia.

Awards

1. **BEST PAPER AWARD**, as co-author of the paper "A Compact Model of Hafnium-Oxide-Based Resistive Random Access Memory," *F. M. Puglisi, P. Pavan, A. Padovani, and L. Larcher, International Conference on IC Design and Technology (ICICDT), Pavia, Italy*.
2. **BEST PAPER AWARD**, as the second author of the paper "Spatio-Temporal Defect Generation Process in Irradiated HfO_2 MOS Stacks: Correlated Versus Uncorrelated Mechanisms," *Fernando Leonel Aguirre, Andrea Padovani, Alok Ranjan, Nagarajan Raghavan, Nahuel Vega, Nahuel Müller, Sebastián Matías Pazos, Mario Debray, Joel Molina, Kin Leong Pey, and Félix Palumbo*, presented at the 2019 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 31 March-4 April 2019. DOI: https://doi.org/10.1109/IRPS.2019.8720539.
3. On June 9th, 2023 I have been awarded the "**2023 Microelectronic Engineering Journal Middle Career Investigator Award and Lectureship**", given by the Elsevier scientific international journal "Microelectronic Engineering" (https://www.sciencedirect.com/journal/microelectronic-engineering/about/awards).
4. **BEST PAPER AWARD**, as the first author of the paper "Towards a Universal Model of Dielectric Breakdown," *Andrea Padovani, Paolo La Torraca, Jack Strand, Alexander Shluger, Valerio Milo and Luca Larcher*, that I presented at the 2023 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 26-30 March 2023. DOI: https://doi.org/10.1109/IRPS48203.2023.10117846.
5. **BEST STUDENT PAPER AWARD**, as the second author of the paper "The Major Effect of Trapped Charge on Dielectric Breakdown Dynamics and Lifetime Estimation," *Sara Vecchi, Andrea Padovani, Paolo Pavan, and Francesco Maria Puglisi*, presented at the 2023 IEEE International Integrated Reliability Workshop (IIRW), 8-12 October 2023. Stanford Sierra Conference Center, Fallen Leaf Lake, CA, USA. DOI: https://doi.org/10.1109/IIRW59383.2023.10477693.
6. **BEST STUDENT PAPER AWARD**, as the second author of the paper "Enhanced Memory Performance in Ferroelectric NAND Applications: The Role of Tunnel Dielectric Position for Robust 10-Year Retention," *Prasanna Venkatesan* et al., presented at the 2025 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2025, pp. 1-7, DOI: https://doi.org/10.1109/IRPS48204.2025.10982749.

Patents

1. US patent US 11158791 B2, "MIEC and tunnel-based selectors with improved rectification characteristics and tunability," granted on October 26, 2021. https://patents.google.com/patent/US20220059764A1/en

International Conferences Organization

1. (2024 – present) member of the Management Committee of the IEEE International Reliability Physics Symposium (IRPS) with the role of Communications Chair (2025) and Exhibitors Chair (2026). https://www.irps.org/committee
2. (2023 – present) member of the Management Committee of the IEEE International Integrated Reliability Workshop (IEEE IIRW) with the role of Poster Chair (2023), Discussion Group Chair (2024), Communications Chair (2025) and Publications Chair (2026)

   https://www.iirw.org/committees

Participation to Technical Committees of International Conferences

I have been and still am part of technical committees of international conferences:

1. IEEE International Reliability Physics Symposium (IRPS). Member of the *Gate Dielectrics* committee (2013-2015) and of the *Gate/MOL Dielectrics* committee (2019-2023), with the role of Vice-Chair (2021), Chair (2022) and Chair Emeritus (2023).

2. IEEE International Integrated Reliability Workshop (IIRW). Member of the technical committee for several years (2012-2015, 2017, 2019 e 2020).
3. International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA). Member of the *Europe subcommittee* from 2012 to 2019.
4. European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF). Member of different committees from 2015 to 2020 and in 2024.
5. IEEE Electron Devices Technology and Manufacturing (EDTM). Member of the Devices and Circuit Reliability (DCR) committee in 2024. Member of the Reliability and Testing committee in 2025.
6. IEEE International Electron Device Meeting (IEDM). Member of the Reliability of Systems and Devices (RSD) committee in 2024 and 2025.

I declare that all content relating to qualifications, publications and activities carried out, reported in the curriculum are true.

Reggio Emilia, 16/09/2026

Andrea Padovani